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EXAMINER	
NATNAEL, PAULOS M	

ART UNIT	PAPER NUMBER
2614	8

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,990	KEATING ET AL.	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-40 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 23-37 is/are allowed.

6)☒ Claim(s) 1-4,6,8-11,13-16,18-21 and 38-40 is/are rejected.

7)☒ Claim(s) 5,7,12,17 and 22 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. There are two claims designated as "claim 38". The first one (on page 26) is an independent claim 38. The second one (on page 27) comes after claim 39 and before claim 40 and is dependent on claim 36. Thus, the second claim 38 has not been considered as to its merits. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims **38-40** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The specification discloses that the counter 110 includes base signal current duration counter 350 and periodic signal continuation device 360 that output a count. In claim **38**, however, while it is claimed that the counter is to receive the second signal and to output a count related to a duration of the second signal, it is not clear whether the output count signal outputted from the counter is used anywhere at all, rendering the claim indefinite.

Claims **39** and **40** are rejected as being dependent on the rejected base claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims **1-4, 8-11,13-16, and 18-21** are rejected under 35 U.S.C. 102(e) as being anticipated by Kobayashi et al., U.S. Patent No. 6,088,323.

Considering claim **1,** Kobayashi et al disclose all claimed subject matter, note;

a) a rising edge corrector to receive jittered signal and to output a jitter corrected rising edge of the jittered signal, is met by the Rising Edge Correction circuit 17A, fig.1;

b) a falling edge corrector to receive the Jittered signal and to output a jitter corrected falling edge of the jittered signal, is met by the Falling Edge Correction circuit 17B, fig.1;

c) an output device to receive the jitter corrected rising edge, to receive the jitter corrected falling edge, and to output a jitter corrected signal, is met by Flip/Flop 25, fig.1, which receives the SS and SR signals and outputs an S5 signal. ((see also col. 5, line 1 to col. 6, line 10)

Considering claim **2**, the apparatus of claim 1 wherein the rising edge corrector further comprises a rising edge detector to receive the jittered signal and to detect a rising edge of the jittered signal, wherein the falling edge corrector further comprises a falling edge detector to receive the jittered signal and to detect a falling edge of the jittered signal, is **inherent** because the corrector would not be able to correct the rising and falling edge signals without first detecting or determining the position or other characteristics of the signals. (see also Figs.2A-D and 3)

Considering claim **3**, the apparatus of claim I wherein the rising edge corrector further comprises a rising edge adjuster to receive the jittered signal and to adjust a rising edge of the jittered signal; and wherein the failing edge corrector further comprises a falling edge adjuster to receive the jittered signal and to adjust a falling edge of the jittered signal, is inherent in the edge correction circuits 17A and 17B, because correcting implies or entails somehow adjusting the rising edge and falling edge signals. (see col. 5, lines 1-9 as well)

Considering claim **4,** the apparatus of claim I further comprising a counter to receive a base signal and to output a count of the base signal, is met by character generating table 51 (fig.6 and 7) which includes counters 53 and 54, fig.7, receives the FG signal and outputs an SCI signal which in turn is used in the data selection to select one of the correction signals; (see also col. 10, lines 33-36)

Considering claim **8**, Kobayashi et al disclose all claimed subject matter, note;

a) rising edge correction means for receiving a jittered signal and for outputting a jitter corrected rising edge of the Jittered signal, is met by the Rising Edge Correction circuit 17A, fig.1;

b) falling edge correction means for receiving the jittered signal and for outputting a jitter corrected falling edge of the jittered signal, is met by the Falling Edge Correction circuit 17b, fig.1;

c) jitter corrected output means for receiving the jitter corrected rising edge, for receiving the jitter corrected falling edge, and for outputting a jitter corrected signal, is met by Flip/Flop 25, fig.1, which receives the SS and SR signals and outputs an S5 signal. (see also col. 5, line 1 to col. 6, line 10)

Considering claim **9**, the apparatus of claim 8 wherein said rising edge correction means further comprises rising edge detection means for receiving, the jittered signal and for detecting a rising edge of the jittered signal.

See rejection of claim 2;

Considering claim **10**, the apparatus of claim 8 wherein said rising edge correction means further comprises rising edge adjuster means for receiving the jittered signal and for adjusting a rising edge of the jittered signal.

Regarding claim 10, see rejection of claim 3;

Considering claim **11**, the apparatus of claim 8 further comprising counter means for receiving a base signal and for outputting a count of the base signal.

Regarding claim 11, See rejection of claim 4;

Claim **13** is a method claim of claim 1 and, thus, claim **13** is rejected for the same reasons as those in claim 1;

Considering claim **14**, the method of claim 13 wherein correcting a rising edge further comprises detecting a rising edge of the jittered signal.

See rejection of claim 2;

Considering claim **15**, the method of claim 13 wherein correcting a rising, edge further comprises adjusting a rising edge of the jittered signal.

Regarding claim 15, see rejection of claim 3;

Considering claim **16**, the method of claim 13 further comprising determining a count of a current duration of a base signal.

Regarding claim 16, see rejection of claim 4;

Considering claim **18,** see rejection of **c**laim **13.**

Considering claim **19**, the medium of claim 18 wherein the instructions, when executed, cause the system to perform correcting by detecting a rising edge of the jittered signal.

Regarding claim 19, see rejection of claim 2;

Considering claim **20**, the medium of claim 18 wherein the instructions, when executed, cause the system to perform correcting by adjusting a rising edge of the jittered signal.

Regarding claim 20, see rejection of claim 3;

Considering claim **21**, the medium of claim 18 wherein the instructions, when executed, cause the system to perform correcting by determining a count of a base signal.

Regarding claim 21, see rejection of claim 4;

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim **6** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al., U.S. Patent No. 6,088,323

Considering claim **6,** the apparatus of claim 1, wherein the Jittered signal further comprises a video signal.

Regarding claim 6, Kobayashi discloses optical disk recording device and method. Optical disks such as compact disc or the DVD are well known for storing both audio and video signals. Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the system of Kobayashi et al by providing video signal in the optical disk recording in order for the system to be able to correct jitter in the video signal as well, so that the system is made versatile and more useful for the consumer.

Allowable Subject Matter

8. Claims **23-37** are allowable over the prior art.

9. Claims **5,7,12,17,22** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claim **38** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

11. Claims **39** and **40** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose an apparatus comprising a rising edge corrector and a falling edge corrector, wherein the rising edge corrector is configured to correct a rising edge of the jittered signal using a count received from the counter, as in claim **5,12,17 and 22**; wherein the jittered signal further comprising a deserialized signal derived from a serialized signal, as in claim **7**.

Wherein the falling edge corrector is configured to correct a falling edge of the Jittered signal using the count received from the counter, a rising edge position adjuster to receive the detection of the rising edge from the rising edge detector, to receive the count from the counter, to determine a rising edge count, to determine whether the rising edge count is within a programmed rising edge window, and to output a center position of the rising edge window as a jitter corrected rising edge position; and, a falling edge position adjuster to receive the detection of the falling edge from the falling edge detector, to receive the count from the counter, to determine a falling edge count, to determine whether the falling edge count is within a programmed falling edge window, and to output a center position of the falling edge window as a jitter corrected falling edge position; a jitter corrected signal output device to receive the jitter corrected rising edge position from the rising edge position adjuster, to receive the jitter corrected falling

rising and falling edges as a jitter corrected signal by using the count from the counter, as in claim **23**;

A counter to receive a base signal and to output a count of the duration of the base signal; a rising edge corrector to receive the jittered signal, to receive the count from the counter, to determine a rising edge count, to output the rising edge count as a jitter corrected rising edge position of the jittered signal if the rising edge count is not within a rising edge programmed window, and to output the center of the rising edge programmed window as the jitter corrected rising edge position of the jittered signal if the rising edge count is within the rising edge programmed window; falling edge corrector to receive the jittered signal, to receive the count from the counter, to determine a falling edge count, to output the falling edge count as the jitter corrected falling edge position of the jittered signal if the falling edge count is not within a falling edge programmed window, and to output the center of the falling edge programmed window as the jitter corrected falling edge position of the jittered signal if the falling edge count is within the falling edge programmed window; and a jitter corrected signal output device coupled to receive the jitter corrected rising edge position from the rising edge corrector, to receive the jitter corrected falling edge position from the falling edge corrector, and to output a jitter corrected signal, as in claim **28**;

Counting a duration of a base signal, when a rising edge of the jittered signal occurs, determining a rising edge count based on the count of the duration of the active state of the base signal; determining whether the rising edge count is within a rising

edge window; if the rising edge count is within a rising edge window, then outputting the center of the rising edge window as a jitter corrected rising edge position or otherwise outputting the rising edge count as the jitter corrected rising edge position; when the falling edge of the jittered signal occurs, determining a falling edge count based on the count of the duration of the active state of the base signal; determining whether the falling edge count is within a falling edge window; the falling edge count is within a falling edge window, then outputting the center of the falling edge window as a jitter corrected falling edge position or otherwise outputting the falling edge count as the jitter corrected falling edge position; outputting a jitter corrected signal by matching the count from the counter with the respective jitter corrected rising edge and falling edge positions, as in claim **34**;

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsuchiya et al., U.S. Patent No. **6,256,003** discloses a jitter correction circuit and a flat panel display device using the same.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Paulos M. Natnael* whose telephone number is (703) 305-0019. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *John Miller* can be reached on (703) 305-4795. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paulos Natnael
February 17, 2004

PAULOS M. NATNAEL
PATENT EXAMINER